

2500A/1200V Dual IGBT Module

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2500A/1200V Dual IGBT Module

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Abstract

A 2500A/1200V dual IGBT module for industrial use is developed. Small inductance internal wiring structure from P to N terminal is developed for this large current device. Semiconductor chips are arranged for the purpose of increasing the cooling capability. An aluminium base plate with direct bonded insulation substrate is used for the purpose of increasing thermal cycling capability. To achieve a better thermal contact between base plate and cooling fin for this large base area device, the base plate is separated into several sections. The 2500A/1200V dual IGBT module package is also applied for 1800A/1700V dual IGBT module.

1. Introduction

Our conventional IGBT module series named MPD (Mega Power Dual), which includes 1400A/1200V dual, serves to realize the larger power industrial equipment easier. The recent expansion of renewable energy generation systems like wind power and photovoltaic is requesting larger system power. To realize this request more simple, a 2500A/1200V dual IGBT module is developed.

2. Structure

2.1. Terminal layout

The outline of this module is shown in Figure 1. The package length is about twice of the width. The main P and N terminals are located at one side, and the AC terminal is located at the opposite side of the package for convenient inverter stack design. The signal terminals are located in the middle area of the package and thus allow the simple mounting layout of the gate driver board directly on top of the module. It also allows the simple wiring when the driver board is located separately.

2.2. Structure of base plate

As the base plate area is getting larger, it becomes difficult to get a good fitting between base plate and cooling fin. To solve this problem, separated base plate sections are used for this module. The module case consists of two parts in the direction of height to sustain the bending stress caused by the separated base plate sections. This structure allows doing some screening test separately for each base plate section. For this purpose existing test equipment for smaller devices can be used.

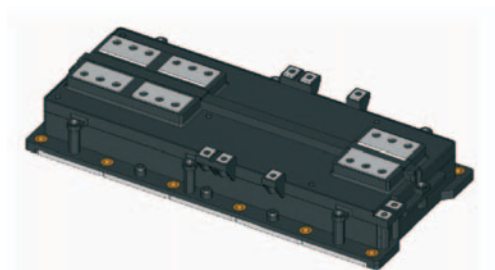


Figure 1: Outline of module

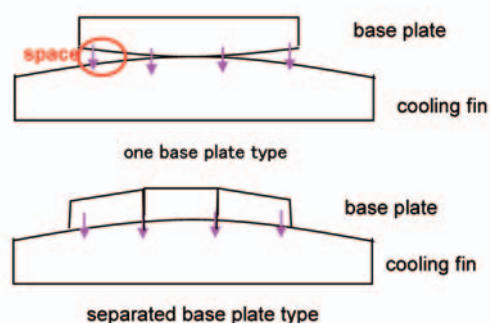


Figure 2: Image of to fit cooling fin

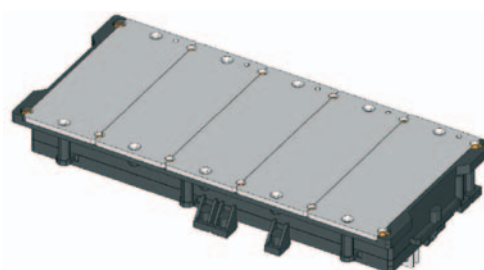


Figure 3: Structure of separated base plate

The total power loss in such large module could be more than 5kW at maximum power in the inverter application. For such high power loss usually liquid cooling will be required. 5000[W/m²K] is one example level for liquid cooling in such applications. For liquid cooling systems the case temperature is changing faster compared with air-cooled systems. Then the thermal cycle capability and thermal radiation ability is important. It will require about 400[cm²] @ΔT_c=25K liquid cooling fin in 5000[W/m²K] condition.

The chosen base plate size of new 2500A/1200V dual module is sufficient for this thermal radiation ability. On the other hand, liquid cooling causes large change of case temperature. It is necessary to increase the thermal cycling capability. To answer this necessity, an aluminium base plate with directly bonded insulation substrate is used (Figure 5). This base plate structure is able to remove the solder layer between base plate and isolation ceramic, which is a weak point for thermal cycling capability in conventional structure of module (Figure 4). This solder layer is subjected to degradation by temperature cycling stress resulting in an increasing thermal resistance R_{th(j-c)} over the lifetime of the module. The thermal resistance of conventional copper base plate structure and aluminium base plate structure is compared by using simulation. The cross sections of copper base plate structure and aluminium base plate structure are shown in Figure 4 and Figure 5.

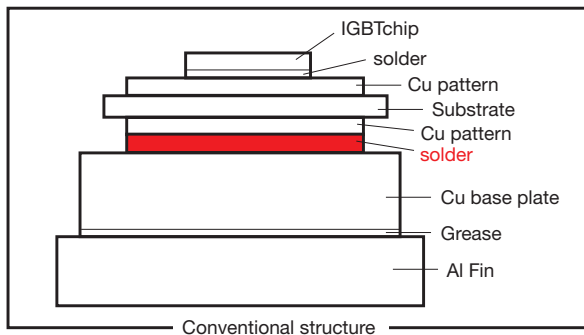


Figure 4: Cross-section of copper base plate structure

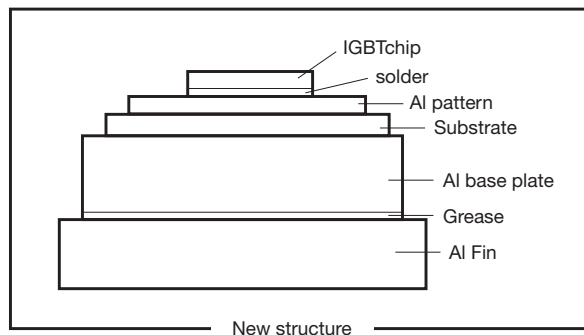


Figure 5: Cross-section of aluminium base plate structure

Figure 6 and Figure 7 show thermal resistance simulation result of copper base plate structure and aluminium base plate structure. The thermal resistance value of copper base plate structure and aluminium base plate structure are almost equal though the thermal conductivity of aluminium is inferior to copper. This results from the elimination of small conductivity solder layer.

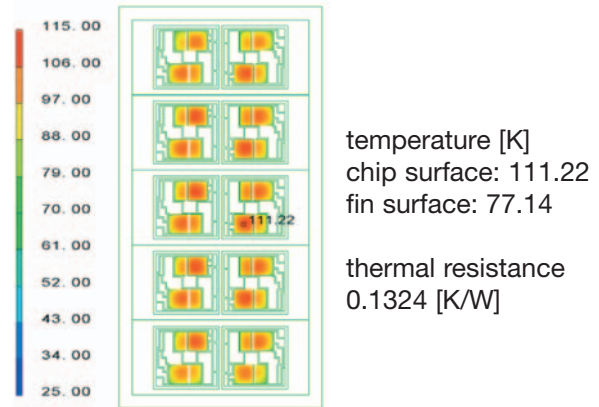


Figure 6: Thermal distribution of chip surface (aluminium base plate)

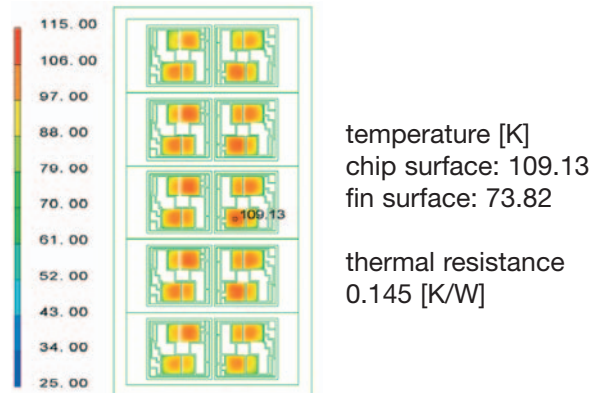


Figure 7: Thermal distribution of chip surface (copper base plate)

2.3. Chip layout

The chip layout was designed for the purpose of increasing the cooling capacity when using liquid cooling. The necessary distance between one chip and another to suppress chip's mutual thermal interference was verified by simulation. Figure 8 shows the structure for this simulation. Figure 9 shows the result of simulation of temperature difference between chip and water at 200[W/chip]. The distance between chips of this module is about 30mm. The result illustrates, that this distance is enough for liquid cooling.

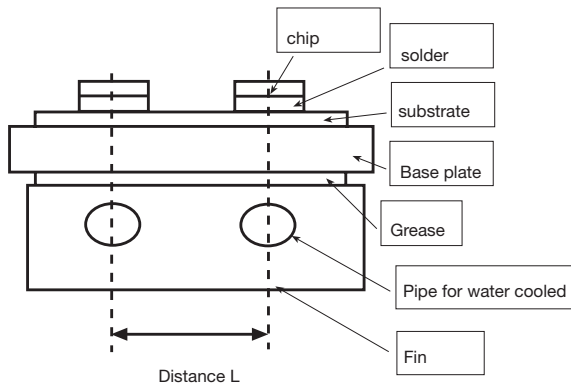


Figure 8: Structure for simulation

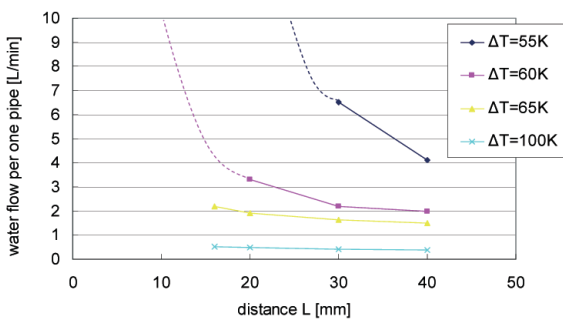


Figure 9: Internal chip distance versus water flow

For best cooling performance the liquid cooling pipe should be located just under the chips. For this purpose the position of base plate mounting holes was chosen to avoid any interference between pipe and mounting hole, see Figure 10.

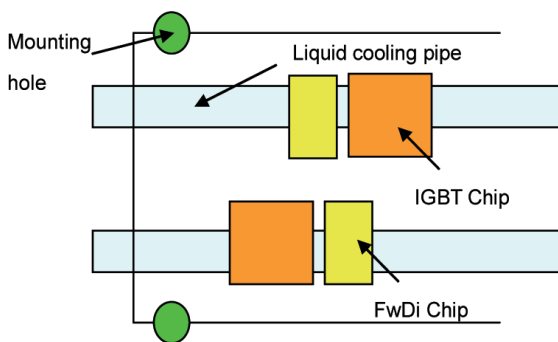


Figure 10: Image of chip layout

2.4. Structure of terminal

Smaller internal package inductance is required when increasing the rated module current. Though the package becomes larger and the length of the wiring tends to become longer when increasing the rated module current thus causing an increase of internal package inductance. This is a trade-off. One way to reduce the inductance per length is to increase the width of the laminated bus inside the module. Though the width is limited by an inside space of the module. To achieve a small inductance bus bar, a four layer laminated bus was selected. This structure allows reducing the concentration of current density in bus bar, and reduces the separation ratio of the current density to each terminal contact by influence the contact of the terminals. The inductance is confirmed by simulation. For adequacy of inductance simulation software against theory, the simulation value is compared with calculation value which calculated by theory equation at simple structure. Figure 11 shows simple structure.

$$\mu_r \mu_0 \times (d/W) \times L$$

- $\mu_r = 1$
- $\mu_0 = 4\pi \times 10^{-7}$
- d : gap of parallel plate (distance)
- W : Direct direction distance of pathway (Width)
- L : Parallel direction distance of current pathway (Length)

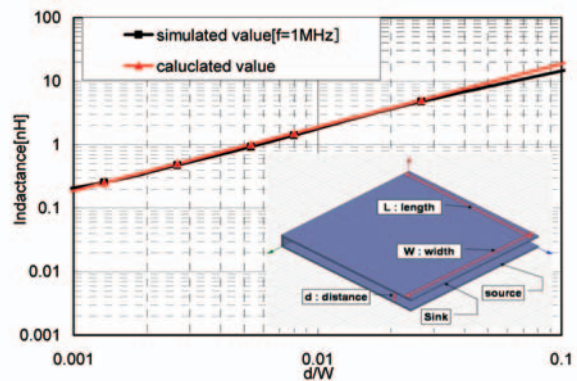


Figure 11: Simulated value versus calculated value

Two results are similar. This simulation is a good method for examination of structure. To achieve a small inside inductance bus bar, four layer laminated bus is used in this package. Figure 12 shows a bus bar structure.

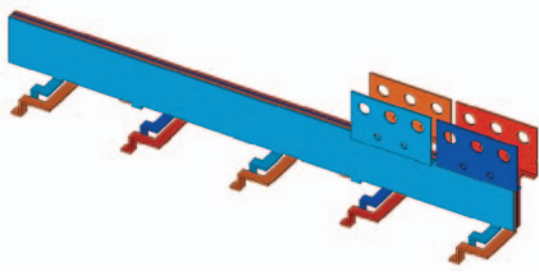


Figure 12: Structure of bus bar

Target inductance of laminated bus part is set to 3nH or less. To realize this value, width of two plate structures are necessary for 50mm or more. As for the case's height, 50mm or less becomes a condition, considering the case strength of transformation. Therefore, two plate structures cannot be achieved. By the simulation, the best structure of parallel plate bar is designed. The simulation value of four parallel plate structures is 2.59nH at 1MHz. This result means four parallel plate structure is a good structure for this module.

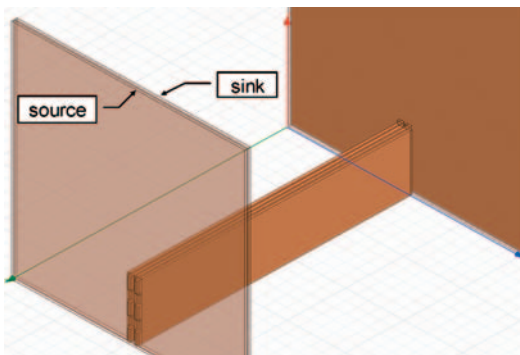


Figure 13: Simulation structure

And this reduction of inside inductance will improve the balance of each chip's current. L2 is small enough compared with L1 and L3. Therefore, the difference of each chip's gate voltage is little. As the result, each chip's current balance is expected to be improved.

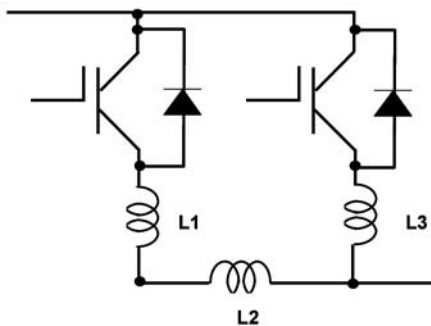


Figure 14: Image of terminal inductance

3. Characteristics

3.1. Inductance of this module

Figure 15 shows the structure of inductance simulation for module. To reject the influence of the outside wiring, a wide laminated bus is connected to the terminals as a source and sink. The sink and source is set to the side of the laminated bus to reduce the influence of the unpractical net surface area.

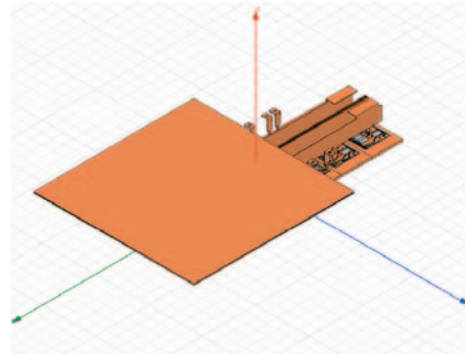


Figure 15: Structure of inductance simulation for module

The simulation result of the total inductance inside the module is 5.18nH from P to N at 1MHz. This result is less than initial target value. Figure 17 shows the test circuit for confirming the internal package inductance. The switching device (CM1400DU-24NF) is switching under the condition of 1500A as a di/dt generator. The DUT (Device Under Test) is connected in series and the voltage peak caused by the impressed di/dt is measured between P and N terminals of DUT. The package inductance of DUT is calculated by using the waveforms shown in Figure 16.

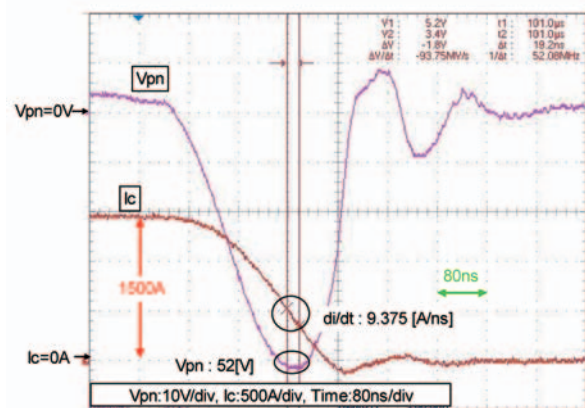


Figure 16: Measurement wave (Vcc = 150V turn-off)

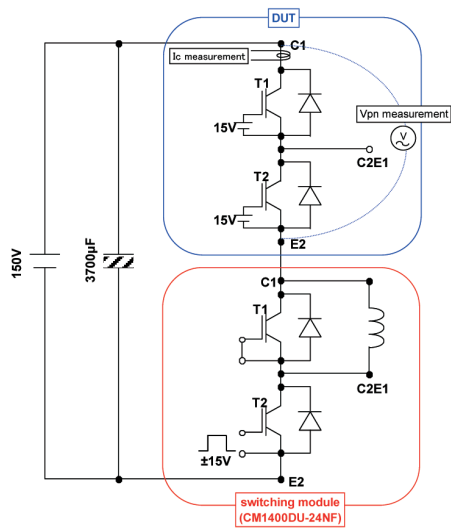


Figure 17: Test circuit

The package inductance inside this module is obtained by the following calculations:

$$\begin{aligned}
 di/dt: & 9.375 \text{ [A/ns]} \\
 V_{pn} \text{ (the generated voltage between P and N):} & 52 \text{ [V]} \\
 V_{ce(sat)}: & 1.37 \text{ [V] @ } I_c=500\text{A} \\
 (V_{pn}-V_{ce(sat)} \times 2) / (di/dt) & = 5.25\text{nH}
 \end{aligned}$$

This value is equal result with simulation value, and the targeted value is achieved.

3.2. Characteristic of 6th generation chip (1200V)

Fine pitch and retrograde profile CS-layer CSTBT is developed as a 6th generation IGBT. Figure 18 shows the cross-sectional view of the 6th generation IGBT and the 5th generation IGBT.

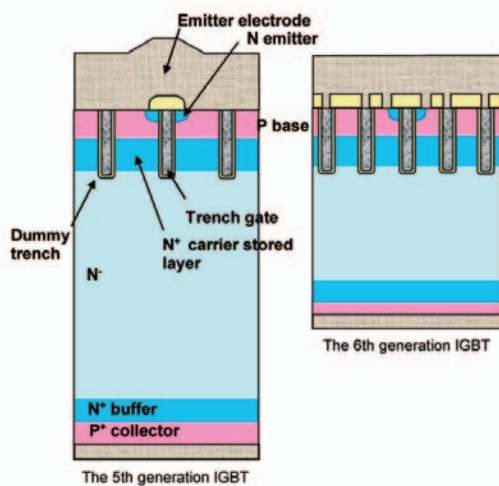


Figure 18: The cross-sectional view of the 6th generation IGBT and 5th generation IGBT

The trade off between $V_{ce(sat)}-E_{off}$ is reduced by 0.7V from our 5th generation at same E_{off} -level. Figure 19 shows the result of one example calculation loss comparison at same dv/dt condition. This shows, that the total loss at inverter operation is calculated as 25% reduced from our 5th generation IGBT module in fixed dv/dt condition.

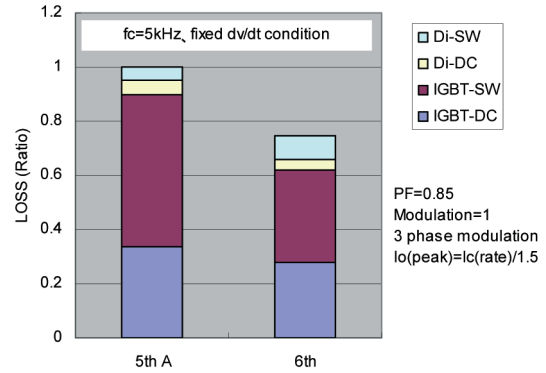


Figure 19: Loss simulation comparison with conventional IGBT module series

3.3. Characteristic of 6th generation chip (1700V)

The same module package is also applied to the newly developed 1800A/1700V dual IGBT module. Therefore, the characteristics of 6th generation IGBT for 1700V are briefly introduced. Figure 20 shows trade off of $V_{ce(sat)}-E_{off}$. The trade off between $V_{ce(sat)}-E_{off}$ is reduced by about 0.35V from our 5th generation at same E_{off} -level. Figure 21 shows turn-on speed control. The turn-on loss is improved by about 25% from our 5th generation at same dv/dt (10kV/µs).

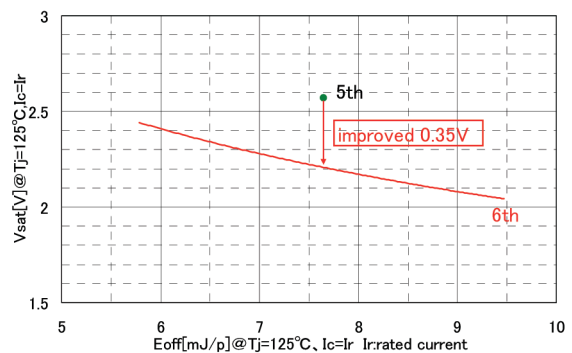


Figure 20: $V_{ce(sat)}-E_{off}$ trade off

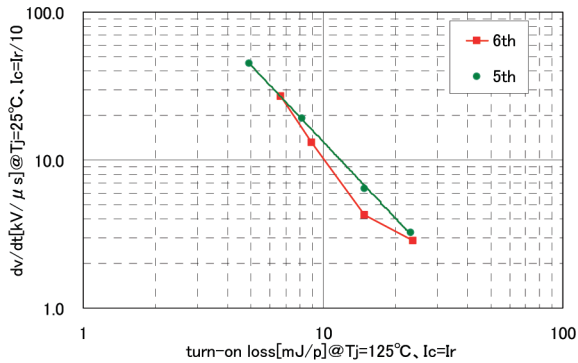


Figure 21: Turn-on loss versus dv/dt

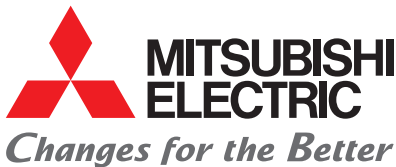
4. Conclusion

A new 2500A/1200V dual IGBT module for industrial use was realized. An extremely low internal package inductance was achieved by using an internal 4-layer main terminal bus. The chip layout is optimized for

liquid cooling. For improved thermal contact resistance to heat sink the base plate consists of several separated sections. Direct bonding between ceramic insulation substrate and aluminium base plate is used for improved thermal cycle capability. Improved loss performance is obtained by using latest 6th generation IGBT and FWDi chips. The same package is also applied to the 1800A/1700V dual IGBT module. And other module ratings are under consideration by using the same standardized base plate section, thus allowing a good cost performance.

5. Literature

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- [2] Tetsuo Takashi: CSTBT™(III) as the next generation IGBT, ISPSD2008-May, pp. 72-75
- [3] Katsumi Satoh: New chip design technology for next generation power module, PCIM 08



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